A 1.75 - 6 GHz MINIATURIZED GaAs FET AMPLIFIER USING QUASI-LUMPED ELEMENT IMPEDANCE MATCHING NETWORKS

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ABSTRACT

A quasi-lumped element impedance matching technique was developed for a multi-octave bandwidth FET amplifier. The lumped elements were realized by parallel capacitors, high impedance band wires and etched lines on a 0.170 x 0.085 x 0.010 inch alumina substrate. A two-stage amplifier has been constructed using this method and yields 17 ± dB gain and 3.5 dB maximum noise figure over 1.75 to 6.0 GHz band.

Introduction

In a broadband FET amplifier circuit design, it is advantageous to use lumped-elements in the impedance matching network and to have the network physically located close to the device. Some circuit designers employ the monolithic integrated circuit approach[1,2,3] to attain the "close-in" matching while some others use MOS or MOM capacitors to realize lumped elements in a so-called hybrid circuit approach.[4,5] The monolithic circuit approach requires a precise "device level" process control and provides no flexibility for any circuit adjustment. The cost of monolithic amplifiers cannot generally be justified without a very large volume. In the hybrid approach MOS or MOM capacitors are incorporated in the circuit either by mounting directly on the ground plane without a substrate or by mounting on top of the substrate with plated thru holes. Either method requires additional fabrication processes as part of the assembly. Futhermore, the MOS and MOM lumped capacitor values are hard to control within a tolerable window and less flexible for circuit tuning. In this report, a quasi-lumped element impedance matching technique will be described for a multi-octave bandwidth FET amplifier. The lumped capacitors were realized as parallel plate capacitors on 10 mil thick alumina substrates and the inductors were approximated by high impedance bond wires or by 1 mil wide etched lines on the substrate. The complete quasi-lumped element impedance matching network can be fabricated by circuit photolithographic methods without using any discrete lumped elements. The fabrication process is greatly simplified.

A 1.75 - 6.0 GHz FET amplifier was designed using this method. The input and the output impedance matching networks were realized individually on two miniature pieces of 0.170 x 0.085 x 0.01 inch alumina substrate. The complete matched amplifier was mounted on a 0.200 x 0.380 inch metal carrier. A two-stage amplifier designed this way was constructed and yields a broadband gain of 17±1 dB and noise figure of 2.8 ± 0.7 dB over the entire designed frequency band.

Amplifier Design

Raytheon's RLC832 1-micron gate length by 500-micron gate periphery low noise FET was used in the circuit design.

To design the input and output matching network the S-parameters of the FET chip were measured on an automatic network analyzer at both maximum gain and minimum noise figure bias (I_{DS} = 15% I_{DSS} for minimum noise figure). A LCL low pass filter type impedance matching network shown in Figure 1 was chosen for broadband input and output matching. The circuit element values required to achieve the desired performance were obtained by CAD using the COMPACT program. Typical capacitance required for an S to C-band amplifier circuit is 0.5 ± 0.2 pf and typical inductance value required range from 1 to 6 nh. It is well known that a series inductance can be approximated by a high impedance transmission line. In our circuit, the lumped-inductance is realized by a 1 mil gold bond wire or by a 1 mil etched line on the substrates. It is also known that if the physical size of the capacitor is much less than a quarter-wavelength, it will behave like a lumped capacitor. For a 10 mil thick alumina substrate (ϵ = 9.8), the parallel plate capacitance between the top and the bottom metalization is calculated to be 0.022 pf per 10 mil square. Therefore, the required area for a 0.5 pf lump-capacitor realized on the 10 mil thick alumina substrate is only in the vicinity of 50 mil square, which is much less than a quarter-wavelength in S, C and even in X-band. It is for this reason that 10 mil thick alumina substrates were chosen for our circuit design. The complete impedance matching network can be realized on a 0.170 x 0.085 alumina substrate without using any discrete components.

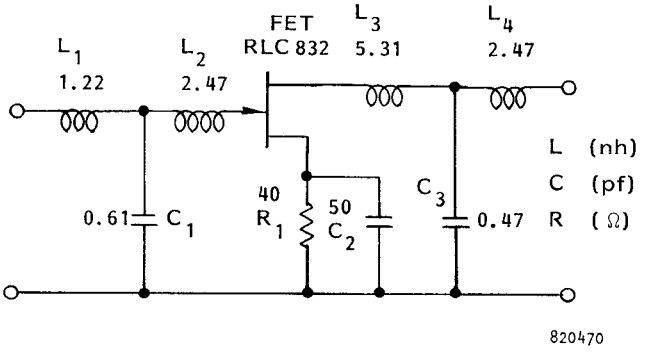

Fig. 1. Equivalent Circuit and Optimized Values of Circuit Elements of a Unit Amplifier.

The GaAs FET gate source capacitance and source drain capacitance can vary by ±10% due to variations in channel doping and gate length[6] resulting from FET processing tolerances. It was therefore felt necessary to realize a circuit with trimming capability. This was done by layout of the amplifier circuit as shown in Figure 2. The inductors in Figure 1 were realized by two or three one mil diameter gold bond wires each. The capacitors were realized by pads (50 mil square) on the substrate. All the bond wires were straight wires to keep the variations in their lengths to a minimum. Tuning can be achieved by changing the bond wire length as shown by the dotted lines. Also capacitance C_1 and C_3 can be increased by bonding one or more small pads near by.

A self biased source resistor is used to obtain minimum noise figure bias at the gate thus eliminating the need for two bias power supplies. The 50 Ω source resistor R_1, the

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bypass capacitor C_2 and GaAs FET are soldered to the gold plated copper carrier resulting in a good RF ground for the source connection. The value of the bypass capacitor C_2 is non-critical and therefore a discrete chip capacitor was used. The complete matched amplifier, including input and output impedance matching networks and the FET with self-biasing, was fabricated on a 0.200 x 0.380 inch carrier.

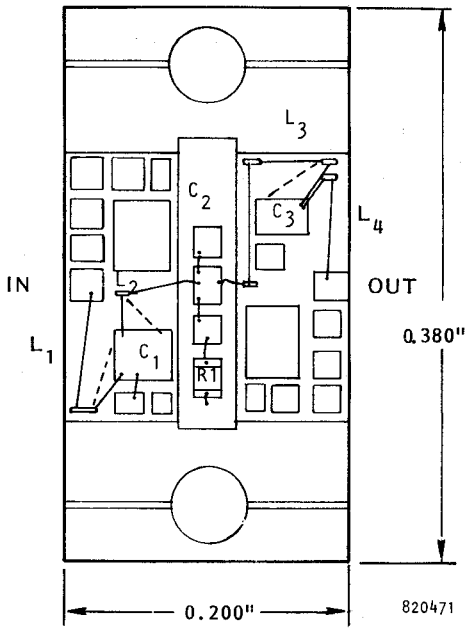

Fig. 2. Layout of the Unit Amplifier with Quasi-Lumped Element Impedance Matching.

The overall amplifier uses a balanced configuration to obtain good input and output VSWR. A pair of matched amplifiers are combined with 3 - dB hybrid couplers. Thus a multi-stage amplifier can be formed by just cascading more stages without any readjustment. The drain bias and the gate ground return in the pair of amplifiers were applied through 10 turn coils to minimize their effect on the circuit. Chip capacitors (~40 pf) mounted on the 3 dB coupler serve as DC blocks. A two-stage cascaded amplifier is shown in Figure 3.

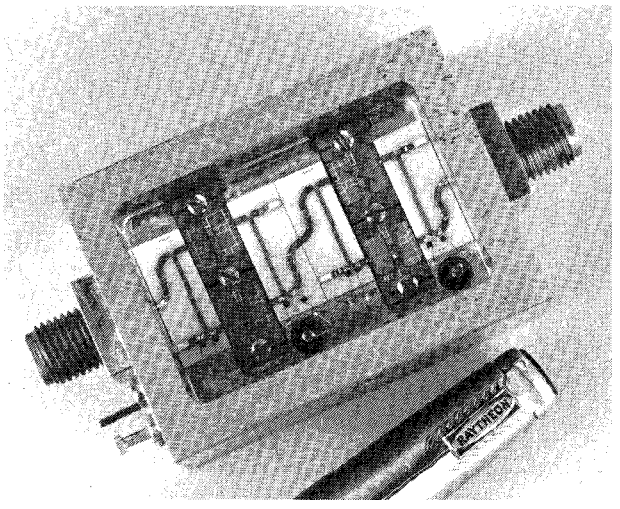

Fig. 3. Photograph of two stage low noise amplifier.

Figure 4 shows the realization of the same impedance matching networks in another manner using spiral inductors and high impedance lines etched on 10 mil thick ceramic substrate. This eliminates the need for coils and bond wires to realize bias chokes and impedance matching lumped inductors. Tuning can still be performed by bonding in more metalization pads to capacitors C_1 and C_3. One mil wide lines, which can be etched by standard photolithography, were used as impedance matching lumped inductors. Bias chokes of 15 nh were formed by four turn spirals with 1 mil wide lines and 2 mil spacing between the lines. The rest of the circuit is the same as described earlier.

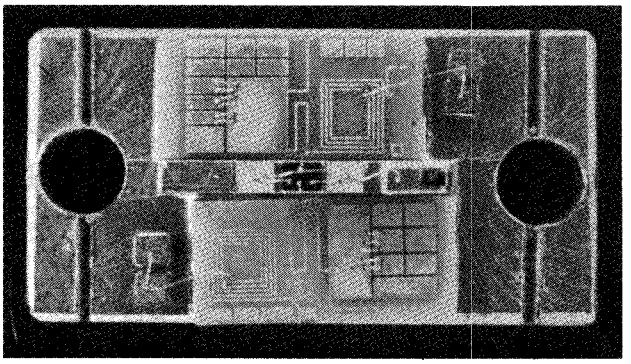

Fig. 4. Photograph of the Unit Amplifier with Etched Spiral Inductors.

Amplifier Performance

Figure 3 shows the photograph of the complete two stage amplifier with a five volt regulator on the bottom side. The overall amplifier size is 1.5 x 1.1 x 0.85 inches and it weighs 50 gms. The amplifier requires 10 v power supply and draws 150 mA current. Figure 5 shows the gain, input and output VSWR of the amplifier shown in Figure 2. The gain of 17 $\pm$ 1 dB is obtained across 1.75 to 6 GHz band. The bandwidth is limited by 3 dB hybrids. At lower frequencies (1.75 - 3 GHz), the 3 dB coupler has more loss, but that is compensated by increased device gain. The input and output VSWR is better than 2:1 (Return loss >10 dB). Since the input of amplifier first stage is matched for minimum noise figure, it is hard to obtain low input VSWR unless the two transistors are well matched (i.e. have same I_{dss} and pinch off voltages). Figure 6 shows the noise figure is below 3.5 dB across 1.75 to 6 GHz band. The noise figure is very sensitive to circuit elements C_1 and L_2 and degrades with increases in C_1 particularly at lower frequencies (2-4 GHz). Gain variation over temperature showed that gain decreased by 1.2 dB as the temperature of the amplifier housing is increased from 25°C to 90°C. The amplifier had minimum saturated power output of +15 dBm.

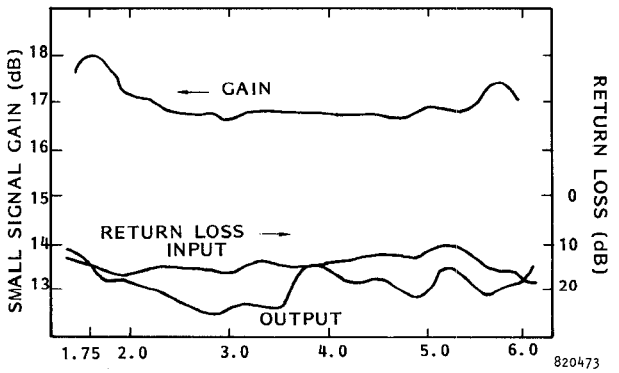

Fig. 5. Gain and VSWR of Two Stage Amplifier.

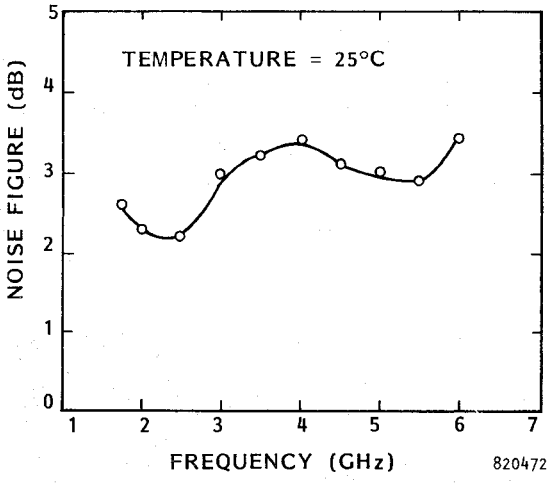

Fig. 6. Noise Figure vs Frequency of Two Stage Amplifier.

Measurements on amplifier of Figure 4 showed similar performance with slightly increased noise figure which may be due to parasitic losses in the etched spiral inductors. Eight dB gain per stage was obtained indicating that inductors realized on a thin (0.010 inch thick) alumina substrate work well in spite of their proximity to the ground plane.

Conclusion

A quasi-lumped element impedance matching network for a multi-octave bandwidth amplifier was developed. The impedance matching network can be realized on 10 mil thick alumina substrates by conventional circuit photolithographic method without using any discrete components. It provides great circuit tunability for various frequency bands from S to C-band and even into X-band. The technique is suitable for low cost and compact size multi- octave bandwidth FET amplifier production.

Acknowledgment

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